VLSI- Design of Integrated Circuits

Winter Term 2006/2007

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http://www.microelectronic.e-technik.tu-darmstadt.de

Organizational (I)

- This lecture is intended for students of the following subjects:
  - Wirtschaftsingenieurwesen Elektrotechnik (FB1, ab 5. Semester)
  - Elektrotechnik und Informationstechnik (FB18, ab 5. Semester)
  - Informatik (FB20, nach dem Vordiplom)
  - Intern. Master Program Information & Communication Engineering
  - Master Program „Informations- und Kommunikationstechnik“

- Requirements: Basics of electronics and communications
  (i.e. lecture „Grundlagen der Elektronik“)

- Courses which are directly founded on this lecture:
  - VLSI-Design Lab. (SS)
  - Microelectronics CAD Lab. (2 weeks, full day course, WS)
  - VHDL-course (1 week) and VHDL-laboratory (2 weeks)(full day course, SS)
  - Computer Aided Design for Integrated Circuits (RSE1, SS)
  - Advanced Methods of Computer Aided Design for Integrated Circuits (RSE2, WS)
Organizational (II)

Lecture:
Monday 14:25h - 16:05h in room S3|06/051 (former 48/051)
Wednesday 11:40h - 13:20h in room S3|06/053 (former 48/053)

Practice:
The excercises will take place within the lecture hours (Mon. or Wed.)

Attending Staff:
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Consultation hours:
On request

Exam

Diploma Exam:
Type: written exam
Date: will be announced by FB18 examination office
Duration: 90 minutes
Allowed materials to use: none
Relevant topics: Topics of lectures and exercises
Overview

- Introduction
- Repetition MOS Devices
- CMOS Inverter
- CMOS Technology
- Static CMOS Logic
- Synchronous Logic
- Basic Sequential Circuits
- Performance
- CAD - Design Flow
- Digital Subsystem Design
- ASIC Design Concepts
- Arithmetic Units
- Micro Architectures
- Memories
- ASIC Design Guidelines
- Design for Testability
- VLSI in Signal Processing
- VLSI in Communications
- Digital Baseband Design

Literature


http://bwrc.eecs.berkeley.edu/Classes/IcBook/index.html