Chapter 20

Boundary-Scan Architecture – JTAG Standard

- miniaturization of electronic components, multilayer and surface mount techniques make test of boards more complicate
  ⇒ requirement of design-integrated test structures

- 1985 first meeting of small group from European electronics companies
- later North American companies joined the group (→ Joint Test Action Group = JTAG)
- results: IEEE Standard Test Access Port and Boundary-Scan Architecture
20.1 Classical Board Test Approaches

Figure 20.1: In-circuit test using bed-of-nails

Figure 20.2: Functional test using board connector
Disadvantages of classical approach:

- high costs for test hardware
- increased density
- not suited for surface mount technology
- modern chip testing techniques as
  - scan path techniques
  - built-in self-test techniques (BIST)/BILBO

are not exploited well
20.2 Introduction to Boundary Scan

Scan-testing at the board-level:

- permits use of automatic test pattern generation tools
- simplification of the hardware of the test equipment

Figure 20.4: Scan design at the board level
Figure 20.5: Testing for interconnection faults

<table>
<thead>
<tr>
<th>Input</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>Expected</td>
<td>Actual</td>
</tr>
<tr>
<td>x1x1x0xxxxx</td>
<td>xxxxxxxx01x1</td>
</tr>
<tr>
<td>x0x0x1xxxxx</td>
<td>xxxxxxxx10x0</td>
</tr>
</tbody>
</table>
Introduction to Boundary Scan

Boundary scan application properties and limitations

- each test vector has to be shifted into scan path
  ⇒ not very suitable for testing the chips themselves because of reduced test rate compared to stand-alone chip testing

- well suited for interconnection testing

- testing of dynamic behaviour impossible

- self-testing ICs: boundary scan can be used to trigger the self-test procedure

Figure 20.6: Testing on-chip logic

<table>
<thead>
<tr>
<th>Input</th>
<th>Expected Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>x10xxxx</td>
<td>xxxxx1xx</td>
</tr>
<tr>
<td>x01xxxxx</td>
<td>xxxxx1xx</td>
</tr>
<tr>
<td>x11xxxxx</td>
<td>xxxxx0xx</td>
</tr>
</tbody>
</table>
20.3 The IEEE Standard 1149.1

20.3.1 IEEE Std 1149.1 Architecture

- **TAP Controller**: responds to the control sequences supplied through the test access port (TAP) and generates the clocks and control signals required for the operation of the other circuit blocks.

- **Instruction Register**: shift register which is serially loaded with instruction for test.

- **Test Data Registers**: Bank of shift registers. The stimuli values required for a test are serially loaded into a test register selected by the current instruction. After execution the results can be shifted out for examination.
20.3.2 Test Access Port

- **Test Clock Input (TCK)**: independent of the system clock; used for synchronization of test operations between various chips on a board

- **Test Mode Select Input (TMS)**: Input for controlling the test logic

- **Test Data Input (TDI)**: Serial input for instruction and test register data

- **Test Data Output (TDO)**: Serial output of instruction or test register data (source selected by TMS code)

- **Optional Test Reset Input (TRST\(^{*}\))**: For test initialization

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Figure 20.8: Test data registers
Figure 20.9: Serial connection of IEEE Std 1149.1-compatible ICs

Figure 20.10: Parallel connection of IEEE Std 1149.1-compatible ICs
Control of the test signals

- by external automatic test equipment (ATE) or

- by on-board bus master chip

Figure 20.11: Use of bus master chip to control IEEE Std 1149.1 chips

20.3.3 TAP-Controller

- 16-state FSM which controls data register (DR) and instruction register (IR) operations

- input signals:
  - TRST*
  - TCK
  - TMS
  - last state (stored in internal FFs)
• output signals:
  – Reset*
  – Select
  – Enable
  – ShiftIR
  – ClockIR
  – UpdateIR
  – ShiftDR
  – ClockDR
  – UpdateDR

20.3.4 The Instruction Register

Figure 20.12: Daisy-chain connection of instruction registers

Figure 20.13: Instruction register
Figure 20.14: An example instruction register cell (stage)
20.3.5 Test Data Registers

Test data registers:

- bypass register (mandatory)
- boundary scan register (mandatory)
- device identification register (optional)

Bypass Register

![Bypass Register Diagram]

Figure 20.15: Example design for bypass register

![Bypass Register Usage Diagram]

Figure 20.16: Use of bypass register
Basic Boundary Cells

Figure 20.17: Provision of boundary-scan cells
Figure 20.18: Basic boundary-scan cell for input pin

Figure 20.19: Basic boundary scan cell for output pin