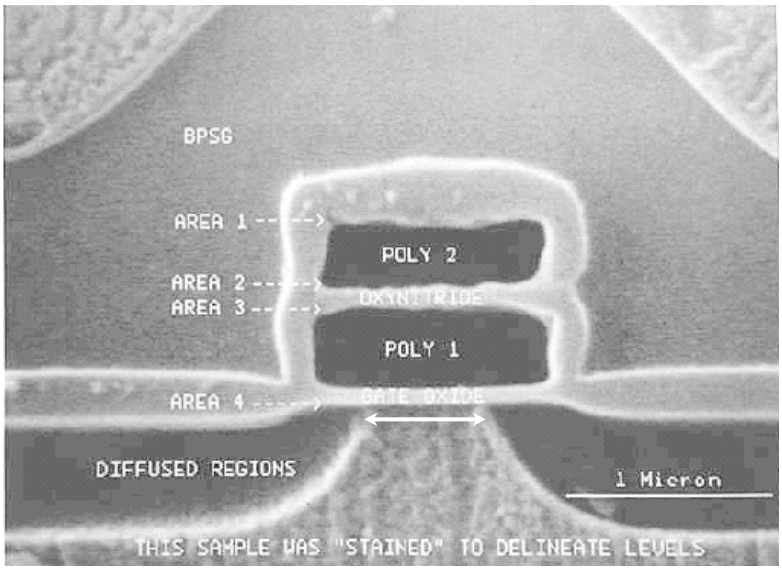
3. Short Channel Effects on MOS Transistors.

MES Institute of Microelectronic Systems

Overview.

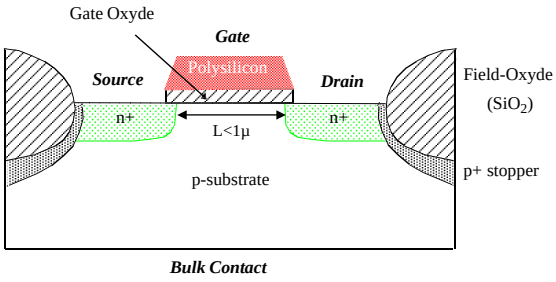
- Short Channel Devices.
- Velocity Saturation Effect.
- Threshold Voltage Variations.
- Hot Carrier Effects.
- Process Variations.



(Source: Jan M. Rabaey, *Digital Integrated Circuits)*

Short Channel Devices.

- As the technology scaling reaches channel lengths less than a micron (L<1µ), second order effects, that were ignored in devices with long channel length (L>1µ), become very important.
- MOSFET's owning those dimensions are called **„short channel devices"**.
- The main second order effects are: Velocity Saturation, Threshold Voltage Variations and Hot Carrier Effects.



CROSS-SECTION of NMOS Transistor

Velocity Saturation Effect (I)

- **Review of the Classical Derivation of the Drain Current:**

$V_{GS}>V_T$

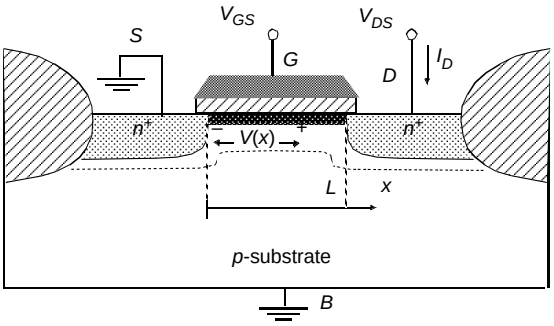
$V_{DS}<<V_{GS}$

- Induced channel charge at $V(x)$:

$$Q_i(x)=-C_{OX}[V_{GS}-V(x)-V_T] \qquad (1)$$

- The current is given as a product of the drift velocity of the carriers v_n and the available charge:

$$I_D=-v_n(x)Q_i(x)W \qquad (2)$$



MOS transistor and its bias conditions

Velocity Saturation Effect (II)

- The **electron velocity** is related to the electric field through **the mobility**:

$$v_n = -\mu_n \mathrm{E}(x) = \mu_n \frac{dV}{dx} \qquad (3)$$

- Combining (1) and (3) in (2):

$$I_D dx = \mu_n C_{OX} W (V_{GS} - V(x) - V_T) dV \qquad (4)$$

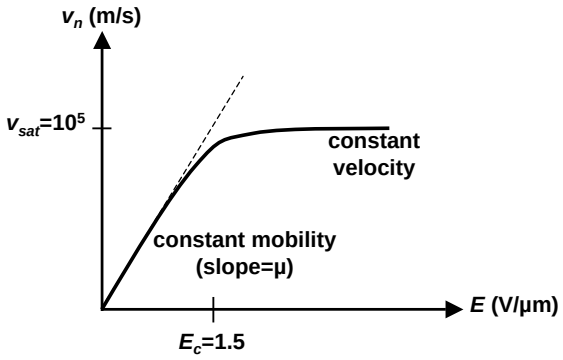
- Integrating (4) from 0 to L yields the voltage-current relation of the transistor:

$$I_D = \mu_n C_{OX} \frac{W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right] \qquad (5)$$

- The behavior of the short channel devices deviates considerably from this model.
- Eq. (3) assumes the mobility μ_n as a constant independent of the value of the electric field E.
- At high electric field carriers fail to follow this linear model.
- This is due to the **velocity saturation** effect.

Velocity Saturation Effect (III)

- When the electric field reaches a critical value $\mathrm{E_C}$, (1.5×10^6 V/m for p-type silicon) the velocity of the carriers tends to saturate (10^5 m/s for silicon) due to scattering effects.



Velocity Saturation Effect (IV)

- The impact of this effect over the drain current of a MOSFET operating in the linear region is obtained as follows:
- The velocity as a function of the electric field, plotted in the last figure can be approximated by:

$$v = \frac{\mu_n \mathrm{E}}{1+\mathrm{E}/\mathrm{E}_C} \quad \text{for } \mathrm{E} \le \mathrm{E}_C \qquad (6)$$

$$v = v_{sat} \quad \text{for } \mathrm{E} \ge \mathrm{E}_C$$

Reevaluating (1) and (2) using (6):

$$I_D = \kappa(V_{DS})\mu_n C_{OX} \frac{W}{L}\left[(V_{GS}-V_T)V_{DS} - \frac{V_{DS}^2}{2}\right] \qquad (7)$$

with:

$$\kappa(V_{DS}) = \frac{1}{1+(V_{DS}/\mathrm{E}_C L)}$$

- For large values of L or small values of V_{DS}, κ approaches 1 and (7) reduces to (5).
- For short channel devices $\kappa<1$ and the current is smaller than what would be expected.

Velocity Saturation Effect (V)

- When increasing the drain-source voltage, the electric field reaches the value E_C, and the carriers at the drain become velocitiy saturated. Assuming that the drift velocity is saturated, from (4) with $\mu_n dV = v_{sat}$ the drain current is:

$$I_{DSAT} = v_{sat} C_{OX} W (V_G - V_T - V_{DSAT}) \qquad (8)$$

Evaluating (7) with $V_{DS}=V_{DSAT}$

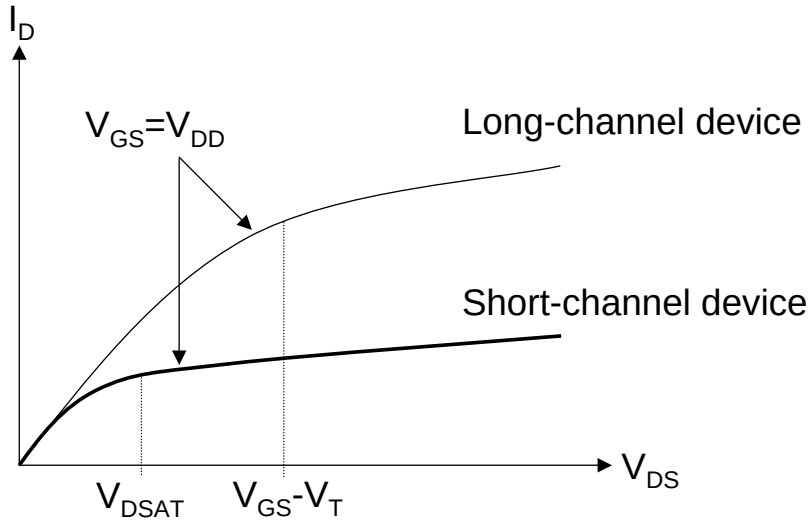
$$I_{DSAT} = \kappa(V_{DSAT})\mu_n C_{OX} \frac{W}{L}\left[V_{GT}V_{DSAT} - \frac{V_{DSAT}^2}{2}\right]$$

- Where V_{GT} is a short notation for $V_{GS}-V_T$.
- Equating (8) and (9) and solving for V_{DSAT}:

$$V_{DSAT} = \kappa(V_{GT})V_{GT} \qquad (10)$$

- For a short channel device and large enough values of V_{GT}, $\kappa(V_{GT})$ is smaller than 1, hence the device enters saturation before V_{DS} reaches $V_{GS}-V_T$.

Velocity Saturation Effect (VI)



Short channel devices display an extended saturation region due to velocity-saturation

Simplificated model for hand calculations (I)

A substantially simpler model can be obtained by making two assumptions:

- Velocity saturates abruptly at E_C and is approximated by:

$\nu=\mu_n E$ for $E \le E_C$

$\nu=\nu_{sat}=\mu_n E_C$ for $E \ge E_C$

- V_{DSAT} at which E_C is reached is constant and has a value:

$$V_{DSAT} = LE_C = \frac{L\nu_{sat}}{\mu_n} \qquad (11)$$

Under these conditions the equation for the current in the linear region remains unchanged from the long channel model. The value for I_{DSAT} is found by substituting eq. (11) in (5).

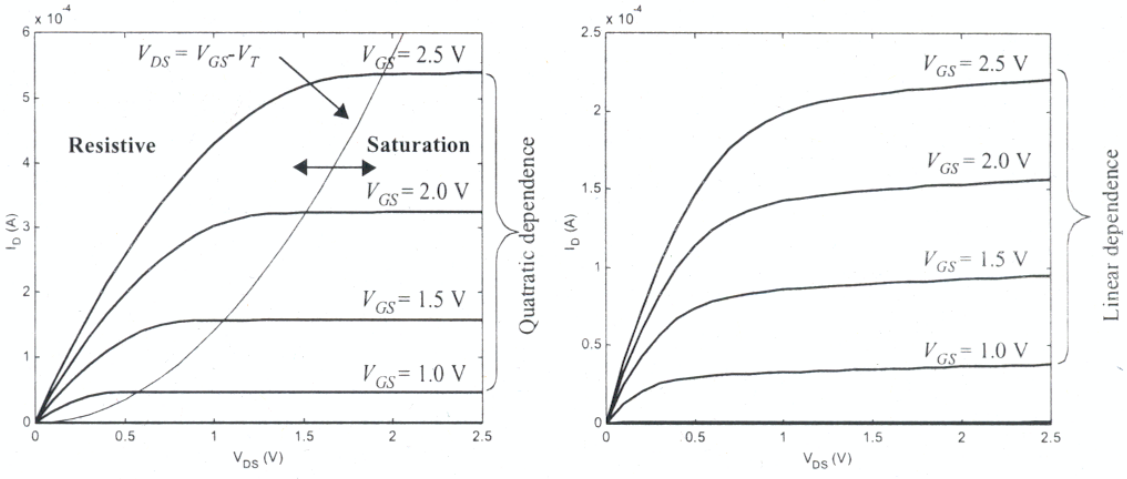
Simplificated model for hand calculations (II)

$$I_{DSAT} = \mu_n C_{OX} \frac{W}{L}\left[(V_{GS} - V_T)V_{DSAT} - \frac{V_{DSAT}^2}{2}\right]$$

$$I_{DSAT} = v_{sat} C_{OX} W\left[(V_{GS} - V_T) - \frac{V_{DSAT}}{2}\right] \qquad (12)$$

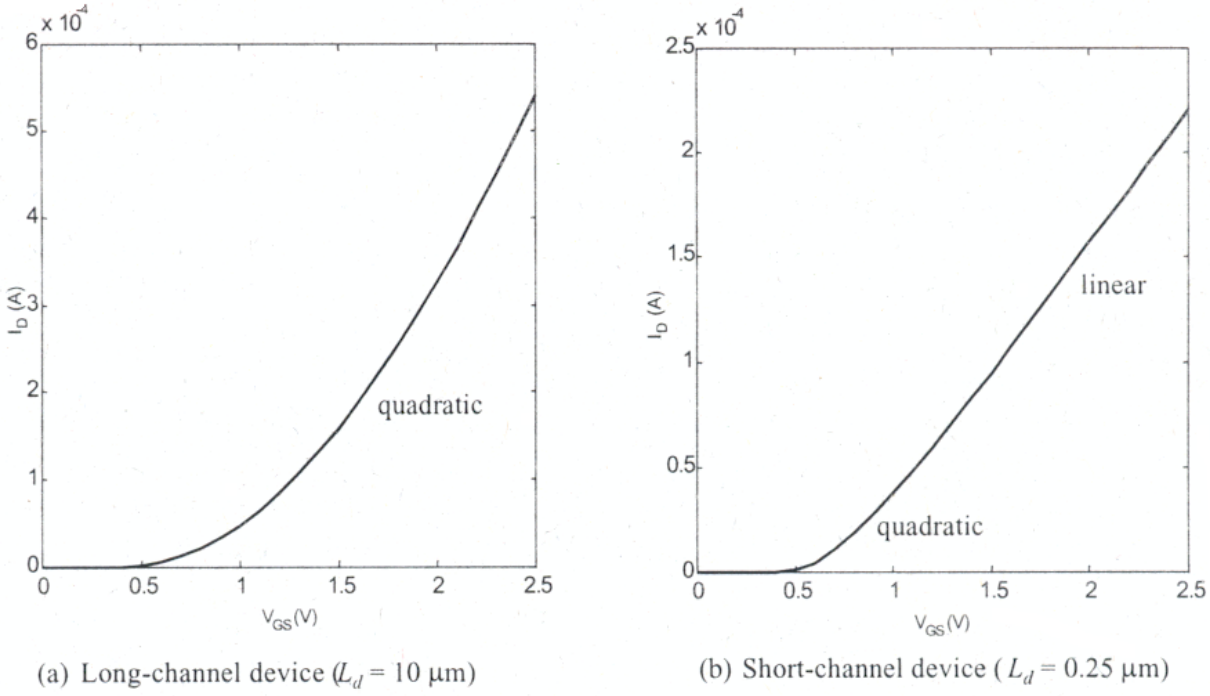
This model is truly first order and empirical and causes substantial deviations in the transition zone between linear and velocity saturated regions. However it shows a linear dependence of the saturation current with respect to V_{GS} for the short channel devices.

I-V characteristics of long- and short-channel MOS transistors both with W/L=1.5



(a) Long-channel transistor (L_d = 10 μm) (b) Short-channel transistor (L_d = 0.25 μm)

I_D-V_{GS} characteristic for long- and short channel devices both with W/L=1.5



(a) Long-channel device (L_d = 10 μm)

(b) Short-channel device (L_d = 0.25 μm)

Threshold Voltage Variations (I)

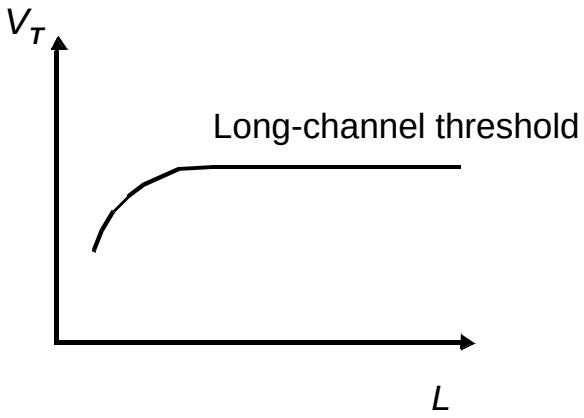
- For a long channel N-MOS transistor the threshold Voltage is given for:

$$V_T = V_{T0} + \gamma\left(\sqrt{\left|-2\phi_F + V_{SB}\right|} - \sqrt{\left|-2\phi_F\right|}\right) \qquad (11)$$

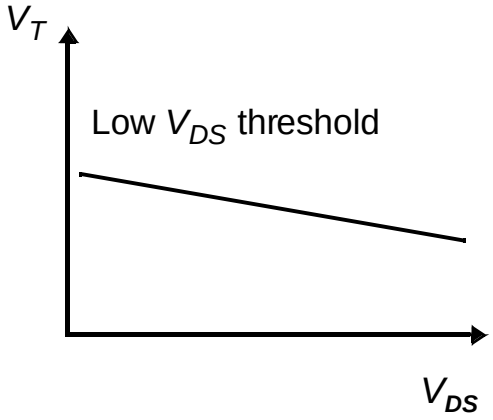
- Eq. (11) states that the threshold Voltage is only a function of the technology and applied body bias V_{SB}

- For short channel devices this model becomes inaccurate and threshold voltage becomes function of L, W and V_{DS}.

Threshold Voltage Variations (II)



Threshold as a function of the length (for low V_{DS})

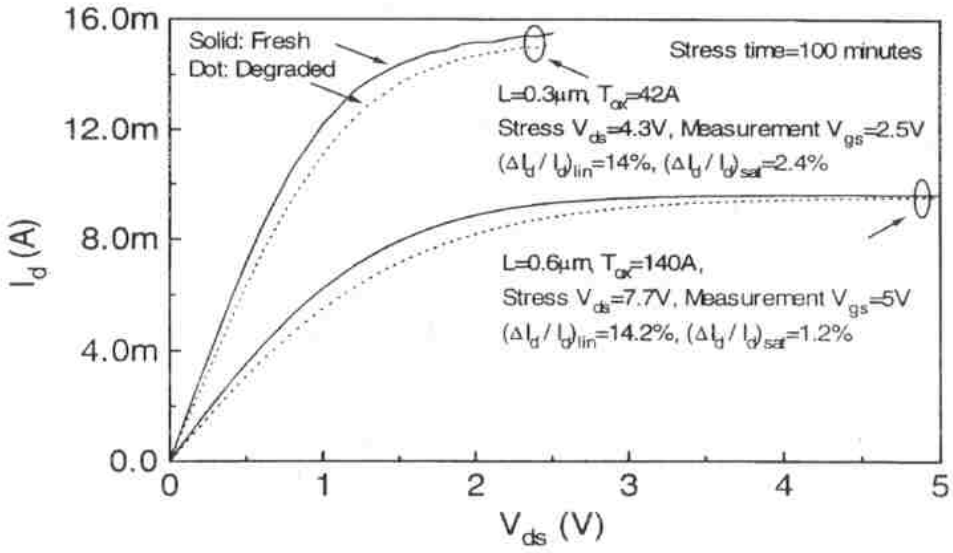


Drain-induced barrier lowering (for low L)

Hot Carrier Effects (I)

- During the last decades transistors dimensions were scaled down, but not the power supply.
- The resulting increase in the electric field strength causes an increasing energy of the electrons.
- Some electrons are able to leave the silicon and tunnel into the gate oxide.
- Such electrons are called „Hot carriers“.
- Electrons trapped in the oxide change the V_T of the transistors.
- This leads to a long term reliabilty problem.
- For an electron to become hot an electric field of 10^4 V/cm is necessary.
- This condition is easily met with channel lengths below 1µm.

Hot Carrier Effects (II)



Hot carrier effects cause the I-V characteristics of an NMOS transistor to degrade from extensive usage.

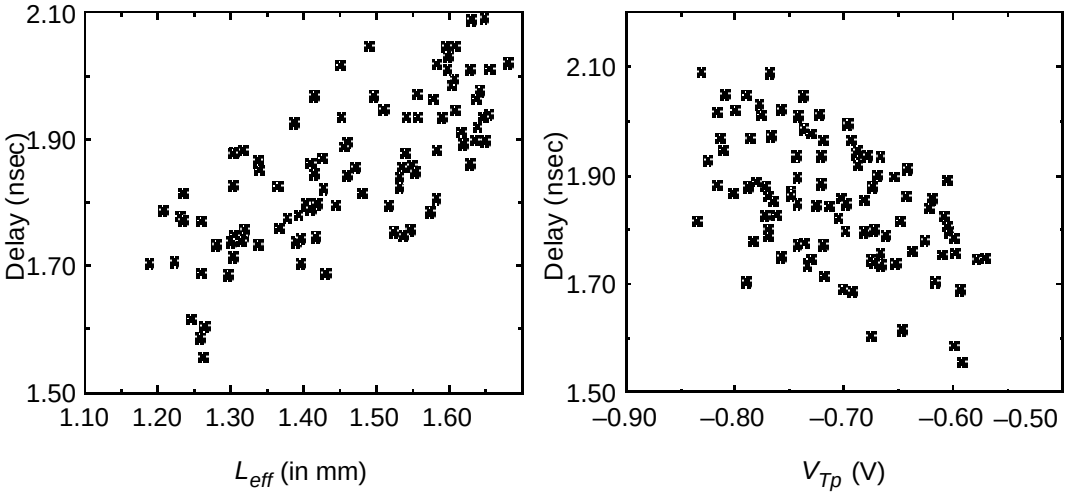
Process Variations.

Devices parameters vary between runs and even on the same die!

Variations in the process parameters , such as impurity concentration densities, oxide thicknesses, and diffusion depths. These are caused by non-uniform conditions during the deposition and/or the diffusion of the impurities. This introduces variations in the sheet resistances and transistor parameters such as the threshold voltage.

Variations in the dimensions of the devices, mainly resulting from the limited resolution of the photolithographic process. This causes (W/L) variations in MOS transistors and mismatches in the emitter areas of bipolar devices.

Impact of Device Variations.



Delay of Adder circuit as a function of variations in *L* and V_T

Parameter values for a 0.25µm CMOS process. (minimum length devices).

	V_{TO} (V)	γ ($V^{0.5}$)	V_{DSAT} (V)	K‘ (A/V^2)	λ (V^{-1})
NMOS	0.43	0.4	0.63	115×10^{-6}	0.06
PMOS	-0.4	-0.4	-1	-30×10^{-6}	-0.1