An illustration of 0.1µm CMOS Layout on PC

Etienne Sicard¹, Sonia Bendhia¹

INSADGEG, 135 Av de Rangueil,
31077 TOULOUSE – France
Email: {etienne.sicard, sonia.bendhia}@insa-tlse.fr
http://intrage.insa-tlse.fr/~etienne

Abstract- The 0.1µm CMOS process technology, in commercial production in 2003, includes copper interconnects, 7 metal layers and five types of MOS devices. In co-operation with ST-microelectronics, the software tool Microwind² has been configured to support this state-of-the-art CMOS process for research and training purpose. This paper describes the recent developments and their application to microelectronics training.

1 Introduction

Most foundries are preparing to offer 0.1µm CMOS process technology in commercial production by end of 2002. This cutting edged process will include copper interconnects, 7 metal layers, three types of oxides and more than four types of MOS devices. Agreements at world-wide scale are being signed to standardise design rules, in order to fit process technologies issued from different foundries.

In co-operation with ST-microelectronics, the software tool Microwind² has been configured to support state-of-the-art CMOS process for research and training purpose. Recently, within the frame of MEDEA+ and IST European research programs [5] the tool has been configured to 0.10µm technology (Figure 1).

![Figure 1. Comparative aspect and performances of Ics in 1992 and 2002](image-url)
2 The CMOS layout editor/simulator

Microwind2 [1] is a user-friendly CMOS circuit editor and simulator tool, for logic and layout level design, running on Windows 98/NT computer. It has been developed since 8 years, and is available as a freeware for educational purpose. Microwind2 gathers a useful set of tools that play an important role in the training in CMOS circuit layout and simulation. Microwind2 allows one to draw the masks of the circuit layout (Figure 2) using a palette of layers. Several layers introduced in 0.1µm (MOS options, salicide options, triple-well) are controlled through the 'option' layer. A built-in device and interconnect extractor is invoked at the press of a single key. Then, the analog simulator uses MOS models 1, 3 or BSIM4 to perform static or time-domain verification of the circuit. The simulator is controlled by properties (ground, supply, clock, pulse, sinus) placed directly on the layout. For educational purpose, a detailed MOS model tutorial is proposed, as well and immediate 2D and 3D views of the circuit. Both logic [2] and analog design [3] of CMOS basic circuits may be conducted easily and successfully with students, during practical training.

Although not supporting very complex layout, and not featuring all possible technological options, Microwind2 is well fitted for fast CMOS layout editing, performance evaluation and small-size circuit prototyping. Microwind2 may compare very easily the performances of the same layout for technologies ranging from 1.2µm down to 0.05µm, a unique feature not provided by any available CAD tool. An e-learning version of Microwind2 is under development to create self animated sequences related to layout-level educational contents.

Figure 2. CMOS layout editing in 0.1µm technology and 2D-section of a portion of circuit
3 A Focus on 0.1µm Features

As new phenomenon and limitation factors did rise in importance with the scaling down of the lithography, the BSIM4 model [4] has been released by the University of Berkeley for accurate modeling of 0.1µm MOS devices. Microwind2 includes a tutorial version of BSIM4, focusing on first-order parameters. In figure 3, the user-interface for displaying the MOS characteristics using BSIM4 is shown for Id/Vd and Id/Vg. The student acts on the model parameters, model option (See section 4) and simulation conditions (Vg,Vd,Vs, Vb, temperature), to observe its consequence on the characteristics and operating point. A dynamic access during simulation is also available.

Figure 3. Simulation of MOS model BSIM4 for 0.1µm devices (Id/Vd, Id/Vg)

The illustration of short channel effects, non-uniform lateral doping effect (Figure 4), or drain-induced barrier lowering is immediately available in the simulation screens of Microwind2.

(a) MOS device with LDD structure  (b) non-uniform lateral doping due to LDD

Figure 4. Effect of non-uniform lateral doping on the threshold

Low-leakage, high speed, ultra-high speed, double-gate and high voltage devices have been made available to address high performance core design, low power system on chip, Flash memories and mixed circuits with the same technology.

Comparative performances of these devices are eased within Microwind. As an example, the simulation of a ring oscillator circuit in 0.1µm CMOS is reported in figure 5. The first simulation concern low leakage MOS devices. When the oscillation is disabled, the stand-by current drops
below 1nA. In high speed mode, the current is higher that 10nA, but oscillates 30% faster (31GHz rather that 23GHz).

Figure 5. Comparative performances of a ring oscillator with different MOS options showing the leakage current increase in high speed mode

4 Training using Microwind2

The tool has been used extensively for introducing CMOS design concepts to student engineers within various institutes and training centre, both academics and industrials. The practical training on CMOS design in 0.1µm has been introduced in December 2001 at ST-University with master students mixed with ST engineers, as well as at our institute. The feedback and evaluation from students has been very positive. Concepts of low power design using MOS options, increased cell density using multiple-layer interconnects, delay and crosstalk have been presented. The corresponding slides are available for free on the web page [1]. The tool Microwind2 should also be available as a companion software of a set of CMOS design text books to appear in the near future, to illustrate and ease the understanding of basic concepts in 0.1µm design and below.

References

5. More information on MEDEA project at www.medea.org