This chapter introduces the CMOS transistor modeling. The static characteristics of n-channel and p-channel MOS devices are shown, with details on the maximum current and its relationship with the sizing, the threshold voltage and various 2nd order effects. Three generations of MOS device models are introduced. Firstly, the original MOS model 1 is presented, as it was proposed in the early versions of SPICE simulator developed by the University of Berkeley, California. This model only applies for long channel devices. Secondly, we introduce the semi-empirical model 3, which is still in use for MOS device simulation with a channel length greater than 1\( \mu \)m. Thirdly, we present a simplified version of the BSMI4 models, developed by the University of Berkeley for MOS devices with channel length down to 100nm. Details on model parameters are provided for all models. The effects of temperature on the MOS performances are then presented. Finally, the three different MOS that may be found in 0.12\( \mu \)m are introduced: low Vt, high speed and high voltage.

1. Introduction to modeling

Modeling the MOS device consists in writing a set of equations that link voltages and currents, in order to simulate and predict the behavior of the single device [Shockley] and consequently the behavior of a complete circuit. A considerable research and development effort has been dedicated in the past years for modeling in an accurate way MOS devices. Many books have been published over the years about the semiconductor physics and semiconductor device modeling. The most common references are [Tsividis], [Sze], [Lee] and recently [Liu]. For MOS devices, one of the key objective of the model is to evaluate the current Ids which flows between the drain and the source, depending on the supply voltages Vd, Vg, Vs and Vb.
From the equation (3-1), we may represent the variation of the current $I_{ds}$ versus voltages in three different ways, as illustrated in figure 3-xxx. The graphs are usually called "$I_d/V_d$", "$I_d/V_g$", and "$I_d(log)/V_g$". For simplicity, we consider that the voltage $V_s$ is grounded.

In the $I_d/V_d$ curve, the current $I_{ds}$ is plotted for varying gate voltage $V_{gs}$, from 0 to $V_{DD}$. The parameter $I_{on}$ gives the maximum available current, corresponding to maximum voltage $V_{ds}$ and $V_{gs}$. $I_{on}$ is a very important parameter for signal switching, for example in logic gates.

In the $I_d/V_g$ curve, we extract the threshold voltage. In the previous chapter we observed the parasitic effects due to this threshold. Analog design is much concerned by an accurate prediction of the threshold voltage.

Then, the curve $I_d(log)/V_g$ is used to build an accurate model of the MOS device for small values of the gate control. One of the most important parameters is the $I_{off}$ current, when $V_g=0$, that has a direct impact on standby power consumption.

A second objective of MOS models is to estimate the value of parasitic capacitances, mainly $C_{gs}$, $C_{gd}$ and $C_{gb}$. Those capacitance prove to vary with the voltage $V_s$, $V_d$, $V_g$, and $V_b$. Although not considered in the static simulations $I_d/V_d$ and $I_d/V_g$, the variation of the capacitance must be computed at each iteration of the analog simulation, for accurate prediction of the switching delay.

\[ C_{gs} = f_1(V_d,V_g,V_s,V_b) \]  
\[ C_{gd} = f_2(V_d,V_g,V_s,V_b) \]  

(eq 3-2)  
(eq 3-3)
A long list of MOS models have been developed for analog simulators. We choose to implement in Microwind2 three of those: the model 1, the model 3 and the model BSIM4. Details on those three models and their physical basis are provided in the next paragraphs.

The complete set of parameters for a given technology is called the model card. The procedure to build an accurate MOS model is quite complex, as it is based on a large set of measurements and sophisticated optimization procedures. The experimental data concerning a MOS device with large width and large length is used first, to fix basic parameters. Then the MOS model is tuned for small channel device measurements, and then for several sizes.

2. MOS Model 1

Equations

Historically, the MOS model 1 was the first to be proposed by Shockley, in 1952 [Shockley]. The equations of the MOS level 1 are provided in the next paragraphs. The evaluation of the current $I_{ds}$ between the drain and the source as a function of $V_d, V_g$ and $V_s$ is summarized in equations 3-5,3-6 and 3-7. The model parameters appearing in the user interface of Microwind2 are written using COURRIER font. The device operation is divided into three regions: cut-off, linear and saturated.
Two main domains are considered in the model: the linear area and the saturated area.

IF $V_{gs}<0$, the device is in cut-off mode.

$$I_{ds} = 0$$  \hspace{1cm} (3-5)

IF $V_{ds} < V_{gs} - V_{TO}$, the device is in linear mode.

$$I_{ds} = U_0 \frac{\varepsilon_0 \varepsilon_{r} W}{\varepsilon_{r} L} ((V_{gs} - v_{t}).(V_{ds} - \frac{(V_{ds})^2}{2}))$$  \hspace{1cm} (3-6)

IF $V_{ds} > V_{gs} - V_{TO}$, the device is in saturated mode:

$$I_{ds} = U_0 \frac{\varepsilon_0 \varepsilon_{r} W}{\varepsilon_{r} L} (V_{gs} - v_{t})^2$$  \hspace{1cm} (3-7)

With:

$$v_{t} = V_{TO} + \gamma \beta (\sqrt{(\Phi + V_{BS})} - \sqrt{\Phi})$$  \hspace{1cm} (3-8)

$\varepsilon_0 = 8.85 \times 10^{-12}$ F/m is the absolute permittivity

$\varepsilon_r = \text{relative permittivity, equal to 3.9 in the case of SiO2 (no unit)}$

<table>
<thead>
<tr>
<th>Mos Model 1 parameters</th>
<th>Typical Value 0.12µm</th>
<th>NMOS</th>
<th>PMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{TO}$</td>
<td>Threshold voltage</td>
<td>0.4V</td>
<td>-0.4V</td>
</tr>
<tr>
<td>$U_0$</td>
<td>Carrier mobility</td>
<td>0.06m²/V-s</td>
<td>0.02m²/V-s</td>
</tr>
<tr>
<td>$TOX$</td>
<td>Gate oxide thickness</td>
<td>2nm</td>
<td>2nm</td>
</tr>
<tr>
<td>$PHI$</td>
<td>Surface potential at strong inversion</td>
<td>0.3V</td>
<td>0.3V</td>
</tr>
<tr>
<td>$\gamma$</td>
<td>Bulk threshold parameter</td>
<td>$0.4 \sqrt{V}$</td>
<td>$0.4 \sqrt{V}$</td>
</tr>
<tr>
<td>$W$</td>
<td>MOS channel width</td>
<td>1µm</td>
<td>1µm</td>
</tr>
<tr>
<td>$L$</td>
<td>MOS channel length</td>
<td>0.12µm</td>
<td>0.12µm</td>
</tr>
</tbody>
</table>

Table 3-1: Parameters of MOS level 1 implemented into Microwind2
Implementation in Microwind

The static characteristics of the MOS model 1 may be obtained using the command Simulate → Mos characteristics available in the main menu of Microwind.

Figure 3-xxx: Access to the static MOS characteristics

Figure 3-xxx: The screen used to simulate the static characteristics of the MOS with model 1 within Microwind2
In the right upper part of the window, select the item "Level 1". The variation of $I_d$ versus the voltage $V_{ds}$, for varying gate voltage $V_{gs}$, is shown by default. The device width is 10µm by default, the channel length is 0.12µm. The parameters $V_{TO}$, $U_0$, $TOX$, $PHI$ and GAMMA are listed in the right part of the window.

Mismatch between simulation and measurements

![Graph showing comparison between simulation and measurement](image)

*Fig.3-xxx: The model 1 predict a current 5 times higher than the measurement in the case of a large channel MOS device ($L=10\mu m$).*

These old equations (1968, in [Shichman]) are not acceptable in 0.12µm. If we consider MOS devices with very long length ($L>10\mu m$), the mismatch between the simulation and the measurement is the order of a factor of five. Let us compare the simulation and the measurement, for a device with a width $W=10\mu m$, and a long channel length $L=10\mu m$, fabricated in 0.12µm CMOS technology, as presented in figure 3-xxx. The measurement "Ne10x10.MES" was downloaded using the button "Load Measurement". This measurement corresponds to a n-channel MOS device with a channel width 10µm and length 10µm, fabricated in CMOS 0.12µm from ST-microelectronics.
The mobility was decreased down to 0.011 to match the measurements.

Access to measurements

Correct match between measurement and level 1

Initially, the simulation and measurement do not correspond at all. The mobility $U_0$ needs to be decreased from its initial value 0.06 down to 0.01. The curves are fitted at the price of an unrealistic change in the mobility parameter.

When dealing with sub-micron technology, the current predicted by model "Level 1" is several times higher than the real-case measurements. This means that several parasitic effects appeared with the technology scale down, most of them tending to reduce the effective current compared to the early modeling equations of the model 1.

3. MOS Model 3

For the evaluation of the current $I_{ds}$ as a function of $V_d$, $V_g$ and $V_s$ between Drain and Source, we commonly use the following equations, close from the SPICE model 3 formulations. The formulations are derived from the model 1 and take into account a set of physical limitations in a semi-empirical way.

Figure 3-xxx: Comparing measured $I_d/V_d$ and level 1 simulations for a $10\times10\mu m$ device result in a surprising similarity (Ne10x10.MES).
One of the most important change is the introduction of \( V_{DSAT} \), a saturation voltage from which the current saturates and do not rise as the LEVEL1 model would do. This saturation effect is significant for small channel length. The main LEVEL3 equations are listed below.

**CUT-OFF MODE.** \( V_{gs} < 0 \)

\[
I_{ds} = 0 \quad \text{(3-xxx)}
\]

**NORMAL MODE.** \( V_{gs} > V_{on} \)

\[
I_{ds} = K_{eff} \frac{W}{L_{eff}} (1 + \kappa A \cdot V_{ds}) V_{de} ((V_{gs} - V_{th}) - \frac{V_{de}}{2}) \quad \text{(3-xxx)}
\]

with

\[
V_{on} = 1.2 V_{th} \\
V_{th} = V_{TO} + \gamma (\sqrt{\Phi I} - V_{bs} - \sqrt{\Phi I}) \\
V_{de} = \text{min}(V_{ds}, V_{dsat}) \\
V_{dsat} = V_{c} + V_{sat} - \sqrt{V_{c}^2 + V_{sat}^2} \\
V_{ds} = V_{gs} - V_{th} \\
V_{c} = V_{MAX} \cdot \frac{L_{eff}}{0.06} \\
L_{eff} = L - 2L_{D}
\]
The formulation of the effective K factor (Equation 3-xxx) includes a mobility degradation factor THETA, which tends to reduce the mobility at high Vgs. The consequence is a reduction of the current $I_{ds}$ as compared to LEVEL1.

$$K_{eff} = \frac{e^2}{\varepsilon_{Si}} \frac{U_0}{TOX \left(1 + THETA(V_{gs} - \text{vth})\right)} \quad (3-xxx)$$

In sub-threshold mode, that is for gate voltage less than the threshold voltage, Vds is replaced by Von in the above equations. An exponential dependence of the current with Vgs is introduced by using the equation 3-xxx. Notice the temperature effect introduced in the denominator nkT.

Without any voltage applied to the gate, the current is no more equal to zero. The current of $I_{ds}$ for $V_{gs}=0$ is called the Ioff current (Figure 3-xxx). Its value in 0.12µm is around $10^{-10}$ A. In contrast, for $V_{gs}=V_{DD}$, the maximum current Ion is the order of several mA ($10^{-3}$ A).

$$I_{ds} = I_{ds}(V_{on},V_{ds}) \exp\left(\frac{q(V_{gs} - V_{on})}{nkT}\right) \quad (3-xxx)$$

Fig.3-xxx: Introduction of an exponential law to model the sub-threshold behavior of the current

**TEMPERATURE EFFECTS**

The MOS device is sensitive to temperature. Three main parameters are concerned: the threshold voltage $V_{TO}$, the mobility $U_0$ and the slope in sub-threshold mode dependent on $kT/q$. Both $V_{TO}$ and $U_0$ decrease when the temperature increases. The physical background is the degradation of mobility of electrons and
holes when the temperature increase, due to a higher atomic volume of the crystal underneath the gate, and consequently less space for the current carriers. The modeling of the temperature effect is as follows:

\[
U_0 = U_0(T=27) \left( \frac{T + 273}{300} \right)^{-1.5} \quad (\text{eq. 3-xxx})
\]

\[
V_T = V_T0(T=27) - 0.002(T - 300) \quad (\text{eq. 3-xxx})
\]

For this \(V_{gs}\), \(I_{ds}\) is independent of the temperature.

Fig. 3-xxx The effect of temperature on the MOS characteristics. In \(I_{ds}/V_{gs}\) mode, a specific \(V_{ds}\) makes the current independent of the temperature.

To obtain the curve of figure 3-xxx, click the icon MOS characteristics, select the curve \(I_{ds}/V_{gs}\), enter the value "0" for the upper limit of \(V_b\), to draw only one single curve and enable the screen memory mode by a click on the icon "Enable Memory". When you change the temperature, the change in the slope and the temperature-independent point appear, as shown in figure 3-xxx.

<table>
<thead>
<tr>
<th>Mos Model 3 parameters</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Parameter</td>
<td>Definition</td>
<td>Typical Value 0.12(\mu)m NMOS pMOS</td>
</tr>
<tr>
<td>(V_{to})</td>
<td>Threshold voltage of a long channel device, at zero (V_{bs}).</td>
<td>0.4V</td>
</tr>
</tbody>
</table>
Table 3-xxx: list of parameters used in the implementation of the model LEVEL3 in Microwind2

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value 1</th>
<th>Value 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>U0 (Carrier mobility)</td>
<td>0.06 m²/V.s</td>
<td>0.025 m²/V.s</td>
</tr>
<tr>
<td>TOX (Gate oxide thickness)</td>
<td>3 nm</td>
<td>3 nm</td>
</tr>
<tr>
<td>PHI (Surface potential at strong inversion)</td>
<td>0.3V</td>
<td>0.3V</td>
</tr>
<tr>
<td>LD (Lateral diffusion into channel)</td>
<td>0.01µm</td>
<td>0.01µm</td>
</tr>
<tr>
<td>GAMMA (Bulk threshold parameter)</td>
<td>0.4 V⁰.⁵</td>
<td>0.4 V⁰.⁵</td>
</tr>
<tr>
<td>KAPPA (Saturation field factor)</td>
<td>0.01 V⁻¹</td>
<td>0.01 V⁻¹</td>
</tr>
<tr>
<td>VMAX (Maximum drift velocity)</td>
<td>150Km/s</td>
<td>100Km/s</td>
</tr>
<tr>
<td>THETA (Mobility degradation factor)</td>
<td>0.3 V⁻¹</td>
<td>0.3 V⁻¹</td>
</tr>
<tr>
<td>NSS (Subthreshold factor)</td>
<td>0.07 V⁻¹</td>
<td>0.07 V⁻¹</td>
</tr>
<tr>
<td>W (MOS channel width)</td>
<td>0.5-20µm</td>
<td>0.5-40µm</td>
</tr>
<tr>
<td>L (MOS channel length)</td>
<td>0.12µm</td>
<td>0.12µm</td>
</tr>
</tbody>
</table>

Microwind User’s Interface

You may understand the action of each parameter by using the screen reported in figure 3-xxx. Each parameter may be changed interactively using cursors, or by entering with the keyboard the appropriate value.

Several screens may be proposed:

- Id vs. Vd, for varying Vg. This is the default screen. Its main interest is the characterization of the Ion current, the maximum current available in the device, for Vd and Vg set to VDD.
- Id vs. Vg, for varying Vb. In this screen, the threshold voltage VTO is characterized, as well as its dependence with the bulk polarization.
- Id vs. Vg, in logarithmic scale. This screen is mandatory to characterize the MOS device in sub-threshold mode, that is for Vgs<Vt. Two of the important parameters are the slope of the current vs. Vgs, and the Ioff current. The Ioff current is the standby current appearing between drain and source for Vgs=0.
- Threshold voltage Vt vs. Length. This screen has been added to illustrate advanced the modeling of deep-submicron effects. With LEVEL 3, Vt is constant for varying length, but is impacted by the bulk voltage.
- Capacitance vs. Vds. This screen illustrates the variation of Cgs and Cgd versus the drain-source voltage.
Fig. 3-xxx. The user interface for investigating the effect of each parameter on the current $I_{ds}$ ($W=10\mu m$, $L=0.12\mu m$)

**Current versus drain-source voltage**

Using the display mode "Id vs. Vd", you may see the effect of parameters $U_0$, $TOX$, KAPPA and VMAX. Basically, the carrier mobility $U_0$ moves the whole curve, as it impacts in an almost linear way the current $I_{ds}$. As $U_0$ is nearly a physical constant, a significant change of mobility has no physical meaning. The oxide thickness $TOX$ does the same but in an opposite way.
A TOX increase leads to a less efficient device, with less current. KAPPA changes the slope of the current when Vd is high, corresponding to the saturation region. Finally, VMAX truncates the curves for low values of Vd, to fit the transition point between the linear and the saturated region (Figure 3-xxx).

**Current versus gate voltage**

The role of VTO and GAMMA can be observed in the figure 3-xxx, using the display mode "\textit{Id vs. Vg}". If we use a long channel device, that is a length much greater than the minimum length, the second order effects are minimized. Act on VTO cursors in order to shift the curves right or left, and GAMMA to fit the spacing between curves. U0 and TOX have also a direct impact on the slope for high Vgs.
Now we focus on a short channel MOS device, for example $W=2\mu m$, $L=0.12\mu m$. Using the same display mode $I_d$ vs. $V_g$, we obtain similar curves as for long-channel device. We observe that the shape of the current is bent. This modification is due to short channel parasitic effects. The parameter THETA is used to bend the current curves at high $V_{GS}$. The MOS model 3 do not provide parameters to account for the $V_{TO}$ dependence with length.

**Current vs Vg in logarithmic scale**

We finally illustrate the role of NSS in the display mode "$I_d(\log)/V_g$" (Figure 3-xxx). The parameter NSS has a direct impact on the slope in sub-threshold mode, that is for $V_{GS}<V_{TO}$. 

---

Fig. 3-xxx. The effects of $V_{TO}$ and GAMMA are illustrated in $I_d/V_g$ mode voltage ($W=10\mu m$, $L=0.12\mu m$)
The slope below $V_{TO}$ is adjusted using NSS. The whole curve is shifted using $V_{TO}$ voltage ($W=10\mu m$, $L=0.12\mu m$).

**Fig. 3-xxx.** In sub-threshold region, the $I_d$ dependence on $V_{gs}$ is exponential. The slope is tuned by parameter NSS. The whole curve is shifted using $V_{TO}$ voltage ($W=10\mu m$, $L=0.12\mu m$).

**Capacitance vs. $V_{ds}$**

The five main capacitance considered in our implementation of MOS model 3 are the gate to bulk capacitance $C_{gb}$, the gate to source capacitance $C_{gs}$, the gate-to-drain capacitance $C_{gd}$, the junction capacitance between source and bulk $C_{sb}$ and the junction capacitance between drain and bulk $C_{db}$.
The variation of the capacitance must be computed at each iteration of the analog simulation, for accurate prediction of the switching delay. In our implementation of MOS level 3, we use the following model, based on the formulations given in [Fjedly]. The parameter $V_{\text{dssat}}$ was given by equation 3-xxx.

\[
C_{\text{GS}} = \frac{2}{3} C_i \left[ 1 - \left( \frac{V_{GS} - V_t - V_{\text{dssat}}}{2(V_{GS} - V_t) - V_{\text{dssat}}} \right)^2 \right] \quad (3-xxx)
\]

\[
C_{\text{GD}} = \frac{2}{3} C_i \left[ 1 - \left( \frac{V_{GS} - V_t}{2(V_{GS} - V_t) - V_{\text{dssat}}} \right)^2 \right] \quad (3-xxx)
\]

\[
C_{\text{GB}} = 0 \quad (3-xxx)
\]

with

\[
C_i = W L \frac{\varepsilon_0 \varepsilon_r}{\text{TOX}} \quad (3-xxx)
\]

$W =$ width of the MOS device (m)

$L =$ length of the MOS device (m)

$\text{TOX} =$ oxide thickness (m)

The two remaining capacitance $C_{\text{DB}}$ and $C_{\text{SB}}$ are junction capacitance. Their model is given by equation:
\[ C_{DB} = \frac{W \cdot L_{drain}}{CJ} \left( \frac{V_{BD}}{PB} \right)^{W_{L}} \]  
\[ C_{SB} = \frac{W \cdot L_{source}}{CJ} \left( \frac{V_{BS}}{PB} \right)^{W_{L}} \]  

where

- \( W \) is the channel width (m)
- \( L_{drain} \) is the Drain length, according to figure 3-xxx (m)
- \( CJ \) is 3x10e-4 F/m2 \(<Liu\ p\ 181>\)
- \( PB \) is the built-in potential of the junction, around 0.8V
- \( MJ \) is the grading coefficient of the junction, around 0.5

\[ \text{Figure 3-xxx: The junction capacitance for drain and source have a significant contribution to the MOS capacitance} \]

4. The BSIM4 MOS Model
A family of models has been developed at the University of Berkeley for the accurate simulation of sub-micron and deep submicron technologies. The Berkeley Short-channel IGFET Model (BSIM) exists in several version (BSIM1, BSIM2, BSIM3). The BSIM3v3 version, promoted by the Electronic Industries Alliance (EIA) is an industry standard for deep-submicron device simulation [Eia].

A new MOS model, called BSIM4 [Bsim4], has been introduced in 2000. A simplified version of this model is supported by Microwind2, and recommended for ultra-deep submicron technology simulation. The complete details on BSIM4 are provided in the excellent book [Liu]. BSIM4 still considers the operating regions described in MOS level 3 (linear for low Vds, saturated for high Vds, subthreshold for Vgs<Vt), but provides a perfect continuity between these regions. BSIM4 introduces a new region where the impact ionization effect is dominant (Figure 3-xxx). In that region, Vds is very high, over the nominal supply voltage VDD. One of the key features of BSIM4 is the use of one single equation to build the current, valid for all operating modes. Smoothing functions ensure a nice continuity between operating domains.

![Figure 3-xxx: The three regions considered in our simplified version of BSIM4](image)

The number of parameters specified in the official release of BSIM4 is as high as 300. A significant portion of these parameters is unused in our implementation. We concentrate on the most significant parameters, for educational purpose. The set of parameters is reduced to around 30.
Effective Channel Length and Width

Once fabricated, the physical length $L_{\text{eff}}$ and width $W_{\text{eff}}$ of the MOS device do not correspond exactly to the initial length $L$ and width $W$ drawn using Microwind2 (Figure 3-xxx). The parameters $L_{\text{INT}}$ and $W_{\text{INT}}$ have been introduced for that purpose, with equations 3-xxx and 3-xxx.
Surface potential and junction depth

The surface potential $\Phi_s$ and junction depth are basic parameters entering into account in the evaluation of the threshold voltage and the global current. The surface potential $\Phi_s$ is defined by equation 3-xxx.

$$\Phi_s = 0.4 + \frac{vt}{q} \ln\left(\frac{NDEP}{ni}\right)$$  \hspace{1cm} (3-xxx)

where $vt$ the thermal voltage given by equation 3-xxx, NDEP is the channel doping concentration for zero body bias (Around $10^{17}$ cm$^{-3}$ in practice), and $ni$ is the intrinsic carrier concentration of Silicon ($ni=1.02\times10^{10}$ cm$^{-3}$ at 300°K). Consequently, the surface potential $\Phi_s$ in deep-submicron CMOS process is around 0.85V.

The thermal voltage is

$$vt = \frac{k_B T}{q}$$  \hspace{1cm} (3-xxx)

$k_B =$ Boltzmann constant = 1.38 x $10^{-23}$ J/K

$T =$ temperature (300°K by default)

$q =$ Electronic charge = 1.60 x $10^{-19}$ C

The built-in voltage of the source/drain junctions is given by equation 3-xxx.

$$V_{bi} = vt \ln\left(\frac{NDEP.NSD}{ni^2}\right)$$  \hspace{1cm} (3-xxx)

where $vt$ the thermal voltage given by equation 3-xxx, NDEP is the channel doping concentration for zero body bias (Around $10^{17}$ cm$^{-3}$ in practice), NSD is the source/drain doping concentration (Around $10^{20}$ cm$^{-3}$ in practice), and $ni$ is the intrinsic carrier concentration of Silicon ($ni=1.02\times10^{10}$ cm$^{-3}$ at 300°K). Consequently, the built-in voltage $V_{bi}$ in deep-submicron CMOS process is around 1.0V.

The depletion depth $X_{dep}$ is computed by equation 3-xxx. It corresponds to the thickness of the region near the N+/P- junction interfaces, as illustrated below.

$$X_{dep} = \sqrt{\frac{2\varepsilon_s \varepsilon_0 (\Phi_s - V_{bi})}{q.NDEP}}$$  \hspace{1cm} (3-xxx)
where \( \varepsilon_{\text{r-si}} \) is the dielectric constant of silicon (11.7), \( \varepsilon_0 \) is the permittivity in vacuum \((8.854 \times 10^{-12} \text{F/m})\), \( \Phi_s \) is the surface potential given by equation 3-xxx, NDEP is the channel doping concentration for zero body bias, \( q \) is the electronic charge \((1.60 \times 10^{-19} \text{C})\), and \( v_{\text{bs}} \) is the bulk-source potential. The typical value of \( X_{\text{dep}} \) is 0.5\( \mu \text{m} \) (Figure 3-xxx).

![Fig. 3-xxx: Illustration of the depletion depth Xdep](image)

### Threshold voltage

The main impact of the threshold voltage \( V_t \) is the \( I_{\text{off}} \) parasitic current, that exhibits an exponential dependence with \( 1/V_t \). A high threshold voltage \( V_t \) leads to a small \( I_{\text{off}} \) current, at the price of a low \( I_{\text{on}} \) current. Low threshold MOS devices consume a very high standby current, which impacts the power consumption of the whole circuit. An accurate prediction of the threshold voltage is a key issue for low power integrated circuit design. The general equation of the threshold voltage is presented in equation 3-xxx.

\[
\begin{align*}
V_{\text{th}} &= V_{THO} + K_1 \sqrt{\left( \Phi_s - V_{bs} - \sqrt{\Phi_s} \right)} - K_2 V_{bs} + \Delta V_{SCE} + \Delta V_{NULD} + \Delta V_{DIBL} \\
&= V_{THO} + K_1 \sqrt{\Phi_s} - K_2 V_{bs} + \Delta V_{SCE} + \Delta V_{NULD} + \Delta V_{DIBL} 
\end{align*}
\]

(3-xxx)

where \( V_{THO} \) is the long channel threshold voltage at \( V_{bs}=0 \) (Around 0.5V), \( K_1 \) is the first order body bias coefficient \((0.5 V^{1/2})\), \( \Phi_s \) is the surface potential given by equation 3-xxx, \( V_{bs} \) is the bulk-source voltage, \( K_2 \) is the second order body bias coefficient, \( \Delta V_{SCE} \) is the short channel effect (SCE <gloss>) on \( V_t \) (Detailed in equation 3-xxx), \( \Delta V_{NULD} \) is the non-uniform lateral doping effect (NULD <gloss>) explained in equation 3-xxx, and \( \Delta V_{DIBL} \) is the drain-induced barrier lowering (DIBL <gloss>) effect of short channel on \( V_t \) (Detailed in equation 3-xxx).

### Short channel effect

The threshold voltage is not the same for all MOS devices. There exist a complex dependence between the threshold voltage and the effective length of the channel. For small channel, the threshold value tends to decrease. The equation 3-xxx is proposed, based on an hyperbolic cosine function.

\[
\begin{align*}
\Delta V_{SCE} &= -\frac{0.5.DV T_0}{\cosh(DV T_1, \frac{V_{bi} - \Phi_s}{L_t} - 1)} \\
&= \frac{0.5.DV T_0}{\cosh(DV T_1, \frac{V_{bi} - \Phi_s}{L_t} - 1)} 
\end{align*}
\]

(3-xxx)
where DVT0 is the first coefficient of short-channel effect on the threshold voltage (2.2 by default), DVT1 is the second coefficient of short-channel effect on the threshold voltage (0.53 by default), Leff is the effective channel length given in equation 3-xxx, and It is the characteristic length, approximated in our implementation to 1/4 of the minimum channel length (0.03 µm for a 0.12µm), Vbi is defined in equation 3-xxx, and Φs is the surface potential given by equation 3-xxx.

The illustration of the effect of ∆VtSCE is proposed in figure 3-xxx. Without taking into account the short-channel effect, the threshold voltage is only dependent on Vbs. It can be seen that Vt increase with Vbs decrease. There is no dependence with the length. When we add the contribution of short-channel effect expressed by equation 3-xxx, the threshold voltage is decreased significantly for small length values.

**Non-uniform lateral doping**

The lateral drain diffusion (LDD) is a technique introduced in recent technologies to reduce the peak channel fields in the MOS channel. The location for high-field parasitic effects is illustrated in the process section of figure 3-xxx (a).
In the cross-section of figure 3-xxx (b), the doping concentration at the corner of the gate is reduced thanks to a lightly doped N-type implantation. The Si3N4 spacer is grown over the gate before the N+ highly doped implantation is performed. Consequently, the high-field effects are moderated. Unfortunately, the threshold voltage exhibits a complex dependence with the channel length, as illustrated in figure 3-xxx (d), compared to (c). For decreasing length, the threshold voltage tends to increase first (due to $\Delta V_{t\text{NULD}}$), before decreasing rapidly due to the short channel effect $\Delta V_{t\text{SCE}}$ described in formula 3-xxx.

A simple formulation of the non-uniform lateral doping is $\Delta V_{t\text{NULD}}$ given below:

$$\Delta V_{t\text{NULD}} = K_1(\sqrt{1 + \frac{LPE0}{L_{\text{eff}}}} - 1)\sqrt{\Phi_s} \quad (3-\text{xxx})$$

**Drain induced barrier lowering**

When we apply a positive voltage on the drain of a long-channel n-MOS device, we observe no significant change in the value of $V_t$. When we do the same for a short-channel n-MOS device, we observe a decrease of the threshold voltage. The physical origin of DIBL is the increase of the depletion layer due to a high value of $V_{\text{drain}}$, that reduces the equivalent channel length, and consequently decreases the threshold voltage [Liu].
A simplified model of the DIBL effect on the threshold voltage is proposed in equation 3-xxx. The parameter ETA0 is the DIBL coefficient in sub-threshold region (default value 0.08), and Vds is the drain-source voltage.

\[ \Delta V_{TDI} = -0.5 \cdot ETA0 \cdot Vds \] (Equ 3-xxx)

**Mobility**

In this paragraph, we introduce the formulations for mobility of channel carriers. The generic parameter is U0, the mobility of electrons and holes. The effective mobility \( \mu_{eff} \) is reduced due to several effects: the bulk polarization, and the gate voltage. The equation implemented in Microwind2 is one of the mobility models proposed in BSIM4, reported in 3-xxx.

\[ \mu_{eff} = \frac{U0}{1 + (UA + UC \cdot V_{bseff})(V_{gsteff} + 2(VTH0 - V_{fb} - \Phi_s))_{E}}, \] (Equ 3-xxx)

where

UA is the low field mobility, in m\(^2\)/V-s. Its default value is around 0.06 for n-channel MOS and 0.025 for p-channel MOS.

UA is the first order mobility degradation coefficient, in m/V. Its default value is around \(10^{-15}\).

UC is the body-effect coefficient of mobility degradation, in m/V\(^2\). Its default value is \(-0.045 \times 10^{-15}\).

VFB is the flat band voltage, in V. It is computed using equation 3-xxx, where \(\Phi_s\) is derived from equation 3-xxx. Its value is around 0.8V.

\[ V_{FB} = VTO - \Phi_s - K1 \sqrt{\Phi_s} \] (Equ. 3-xxx)
TOXE is the oxide thickness, in m. A typical value for TOXE in 0.12µm is 2nm (2.10^{-9}m).

EU is a coefficient equal to 1.67 for n-channel MOS, and 1.0 for p-channel MOS.

The parameter $V_{gsteff}$ is a smoothing function, to ensure continuity between the subthreshold region and the linear region.

$$V_{gsteff} = \max (V_{OFF}, \frac{n.vt \ln (1 + \exp(\frac{V_{gs} - V_{th}}{n.vt}))}{1 + n \exp(-\frac{V_{gs} - V_{th}}{n.vt})}) \quad \text{(Equ 3-xxx)}$$

$$n = 1 + N_{FACTOR} \quad \text{(eq 3-xxx)}$$

A specific parameter $V_{OFF}$ is introduced to account for a specific effect appearing in short-channel device when $V_{gs}$ is negative. Conventional models predict that the current decrease with an exponential law down to zero with decreasing $V_{gs}$. For $V_{gs} < 0$, $I_{ds}$ is supposed to be 0.

In reality, $I_{ds}$ stops decreasing near zero $V_{gs}$, and then tends to increase with negative $V_{gs}$. This effect is called gate-induced drain leakage (GIDL). Consequently, the leakage current $I_{off}$ can be significant when $V_{gs}$ is negative (Quite frequent in logic cells). The $V_{OFF}$ parameter stops the $I_{ds}$ at a certain value, a simplified version of the BSIM4 modeling of the so-called gate-induced leakage current (More info may be found in [Liu]).
The parameter NFACTOR is usually close from 1, meaning that n is close from 2. The effect on NFACTOR is illustrated in the display mode Id. vs. Vg, in logarithmic scale, as illustrated in figure 3-xxx.

\[ E_{sat} = \frac{2V_{sat}}{\mu_{eff}} \]  
\[ V_{dsat} = E_{sat} \cdot \frac{(V_{gsteff} + 2vt)}{(E_{sat} + V_{gsteff} + 2vt)} \]

Again, VdsEff is defined to smooth the evolution from Vds to the saturation voltage Vdsat. The parameter DELTA is fixed to 0.01. The effect of DELTA is shown in figure 3-xxx. With a small value of DELTA (0.001 for example), the transition between linear and saturated region leads to a discontinuity. Experimental measurements show a gradual transition, that is well approximated when DELTA=0.01. A higher value of DELTA would lead to an Ids curve significantly lower than measurements.

\[ V_{dseff} = V_{dsat} - 0.5(V_{dsat} - V_{ds} - \delta + \sqrt{(V_{dsat} - V_{ds} - \delta)^2 + 4\delta V_{dsat}}) \]
Fig. 3-xxx: The smoothing function between linear and saturated regions can be modulated by \( \Delta L \). In Microwind2, \( \Delta L \) is fixed to 0.01.

**Current \( I_{ds} \)**

The current \( I_{ds} \) is computed using one single equation, as described below.

\[
I_{ds0} = \frac{W_{eff}}{L_{eff}} \mu_{eff} \frac{e_{r} \varepsilon}{\varepsilon_{ox}} V_{gs} V_{ds} \left( 1 - \frac{1}{A_{bulk} V_{ds}} \left( 2 V_{gs} + 4 v_{t} \right) \right) \frac{V_{ds}}{1 + \frac{V_{ds}}{\varepsilon_{sat} L_{eff}}} \tag{eq. 3-xxx}
\]

The final current used in analog simulation is:

\[
I_{ds} = I_{ds0} \left( 1 + \frac{V_{ds} - V_{ds}}{V_{ascbe}} \right) \left( 1 + \frac{1}{C_{clm}} \ln \left( \frac{V_{ASAT} + V_{ACLIN}}{V_{ASAT}} \right) \right) \tag{eq. 3-xxx}
\]

Two new terms appear after \( I_{ds0} \). The second term of the current equation accounts for impact ionization. It corresponds to a parasitic current at very high \( V_{ds} \), created by hot electrons and generating supplementary pairs or electrons and holes, when hitting the drain region after acquiring a high energy inside the device channel. The parameter \( V_{ascbe} \) is a voltage below which the impact ionization becomes significant. If \( V_{ascbe} \) is large, \( I_{ds} \) is almost equal to \( I_{ds0} \), meaning that there is no impact ionization effect. If \( V_{ascbe} \) is small, the shape of \( I_{ds} \) is changed for high \( V_{ds} \), as illustrated in figure 3-xxx.
Two parameters affect the shape of the ionization current: PSCBE1 and PSCBE2. The first parameter can be changed interactively on the screen. The voltage \( V_{asbe} \) is determined with the following equations:

\[
V_{asbe} = \frac{L_{eff}}{PSCBE2} \exp\left(\frac{PSCBE1}{V_{ds} - V_{deff}}\right)
\]

with

\[
Litl = \sqrt{\frac{XJ}{XJ \times \varepsilon_{rsi} \times TOXE}}
\]

\( XJ \) is the source/drain junction depth, around 0.1\( \mu \)m (10\(^{-7}\) m)

\( TOXE \) is the oxide thickness, in m (Around 3nm in 0.12\( \mu \)m)

\( \varepsilon_{rsi} \) = relative permittivity of silicon (11.7)

\( \varepsilon_{rsiO2} \) = relative permittivity of silicon oxide (3.9)

The third term of equation 3-xxx accounts for the channel length modulation. An illustration of this phenomenon is provided in figure 3-xxx. It represents the \( I_{ds} \) increase with large \( V_{ds} \). Graphically, \( V_{ACL} \) is equivalent to an Early voltage, that is the value for which the \( I_{ds} \) slope would crosses the horizontal axis for negative \( V_{ds} \). For long channel devices (L=1\( \mu \)m for example), the effect of channel length modulation effect
is small, so $V_{ACL\text{M}}$ has a very high value (10V). For very short channels (0.12µm in the case of figure 3-xxx), a significant channel length modulation effect is observed, and $V_{ACL\text{M}}$ is small.

Fig. 3-xxx: The channel length modulation is significant for short channel devices, and corresponds to the $I_{ds}$ increase at high $V_{ds}$.

Only one new parameter, $P_{CL\text{M}}$, is introduced in the equations. The parameters $V_{AS\text{AT}}$ and $V_{ACL\text{M}}$ are detailed below. The original equations from BSIM4 have been significantly simplified, and some fitting parameters have been ignored. See [Liu] for a description and relevant comments about the original equations.

$$C_{clm} = \frac{1}{P_{CL\text{M}}} \left( l_{eff} + \frac{V_{dsat}}{e_{sat}} \right)$$ (eq. 3-xxx)

$$V_{ACL\text{M}} = C_{clm} \left( V_{ds} - V_{dseff} \right)$$ (eq. 3-xxx)

$$V_{AS\text{AT}} = (e_{sat} l_{eff} + V_{DSSat}) \left( 1 - \frac{A_{bulk} V_{dsat}}{2(V_{gseff} + 2V_{t})} \right)$$ (eq. 3-xxx)
Temperature Effects

Three main parameters are concerned by the sensitivity to temperature: the threshold voltage $V_T$, the mobility $U_0$ and the slope in sub-threshold mode. Both $V_T$ and $U_0$ decrease when the temperature increases. The modeling of the temperature effect in BSIM4 is as follows. In Microwind2, $T_{NOM}$ is fixed to 300°K, equivalent to 27°C. $U_T$ is negative, and set to -1.8 in 0.12μm CMOS technology, while $K_T$ is set to -0.06 by default.

\[
U_0 = U_0^{(T=27)} \left( \frac{T + 273}{T_{NOM}} \right)^{U_T} \quad \text{(eq. 3-xxx)}
\]

\[
V_T = V_T^{(T=27)} + K_T \left( \frac{T + 273}{T_{NOM}} - 1 \right) \quad \text{(eq. 3-xxx)}
\]

A higher temperature leads to a reduced mobility, as $U_T$ is negative. Consequently, at a higher temperature, the current $I_{ds}$ is lowered. This trend is clearly illustrated in figure 3-xxx. The reduction of maximum current is 40% between -30°C and 100°C.
For a short channel n-channel MOS device (L=0.12µm), the result of the parametric analysis illustrates the same trend (Figure 3-xxx). The parametric analysis is conducted as follows: the layout "MosTemperature" is loaded first. The MOS is polarized with a gate always on, the drain at VSS, and the source at VDD. The parametric analysis is launched. In the new window, select the temperature (Upper menu) and the Maximum current (Lower menu). We observe in figure 3-xxx a significant decrease of the Ion current with the temperature.

Fig. 3-xxx Configuring Microwind to display the variations of Ids vs. the temperature
Fig. 3-xxx: The parametric analysis reveals an important decrease of the maximum current \( I_{ds} \) with temperature (MosTemperature.MSK).

Meanwhile, in an opposite trend, the threshold voltage is decreased, as \( K_T1 \) is negative (Figure 3-xxx). Therefore, there exists a remarkable operating point where the \( I_{ds} \) current is almost constant and independent of temperature variation. In 0.12\( \mu \)m CMOS, the \( V_{ds} \) voltage with zero temperature coefficient (ZTC) is around 0.9V, as shown in figure 3-xxx.

Fig. 3-xxx: The effect of temperature on the \( I_{ds} \) current, showing a zero temperature coefficient (ZTC) operating point.
In the sub-threshold region, the impact of temperature is extremely important, as demonstrated in figure 3-xxx. At low temperature the current $I_{ds}$ decreased rapidly down to $10nA$, corresponding to a small off-leakage current. In contrast, at high temperature, not only the threshold voltage is reduced but the sub-threshold slope is flattened, which means an exponential increase of the $I_{off}$ leakage current (figure 3-xxx).

### Table: MOS Model Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>NMOS value in 0.12µm</th>
<th>NMOS value in 0.12µm</th>
<th>Name in RUL file</th>
</tr>
</thead>
<tbody>
<tr>
<td>DVT0</td>
<td>First coefficient of short-channel effect on threshold voltage</td>
<td>2.2</td>
<td>2.2</td>
<td>B4DVT0</td>
</tr>
<tr>
<td>DVT1</td>
<td>Second coefficient of short-channel effect on $V_{th}$</td>
<td>0.53</td>
<td>0.53</td>
<td>B4DVT1</td>
</tr>
<tr>
<td>ETA0</td>
<td>Drain induced barrier lowering coefficient</td>
<td>0.08</td>
<td>0.08</td>
<td>B4ETA0</td>
</tr>
<tr>
<td>LINT</td>
<td>Channel-length offset parameter</td>
<td>0.015-6µm</td>
<td>0.015-6µm</td>
<td>B4LINT</td>
</tr>
<tr>
<td>LPE0</td>
<td>Lateral non-uniform doping parameter at $V_{bs} = 0$</td>
<td>2.35-10</td>
<td>2.35-10</td>
<td>B4LPE</td>
</tr>
<tr>
<td>NFACTOR</td>
<td>Sub-threshold turn-on swing factor. Controls the exponential increase of current with $V_{gs}$.</td>
<td>1</td>
<td>1</td>
<td>B4NFACTOR</td>
</tr>
<tr>
<td>PSCBE1</td>
<td>First substrate current induced body-effect mobility reduction</td>
<td>4.24e8 V/m</td>
<td>4.24e8 V/m</td>
<td>B4PSCBE1</td>
</tr>
<tr>
<td>PSCBE2</td>
<td>Second substrate current induced body-effect mobility reduction</td>
<td>4.24e8 V/m</td>
<td>4.24e8 V/m</td>
<td>B4PSCBE2</td>
</tr>
<tr>
<td>K1</td>
<td>First-order body bias coefficient</td>
<td>0.45 V1/2</td>
<td>0.45 V1/2</td>
<td>B4K1</td>
</tr>
<tr>
<td>K2</td>
<td>Second-order body bias coefficient</td>
<td>0.1</td>
<td>0.1</td>
<td>B4K2</td>
</tr>
<tr>
<td>KT1</td>
<td>Temperature coefficient of the threshold voltage.</td>
<td>-0.06 V</td>
<td>-0.06 V</td>
<td>B4KT1</td>
</tr>
<tr>
<td>NDEP</td>
<td>Channel doping concentration</td>
<td>1.717 cm-3</td>
<td>1.717 cm-3</td>
<td>B4NDEP</td>
</tr>
</tbody>
</table>

Fig. 3-xxx The effect of temperature on the MOS characteristics.
Table 3-xxx List of parameters user-accessible in the BSIM4 implementation in Microwind.

### 5. Specific MOS devices

New kinds of MOS devices has been introduced in deep submicron technologies, starting the 0.18µm CMOS process generation. These MOS devices have specific characteristics which are described in this section.

#### Low leakage MOS

The main objective of the low leakage MOS is to reduce significantly the Ioff current, that is the small current that flows from between drain and source with a zero gate voltage. The price to pay is a reduced Ion current. The designer has the possibility to use high speed MOS devices, which have Ioff high leakage but large Ion drive current. The symbols of the low leakage MOS and the high speed MOS are given in figure 3-xxx.

![Fig. 3-xxx: The low leakage MOS symbol (left) and the high speed MOS symbol (right) (MosOptions.SCH)](image)
Fig. 3-xxx: The low leakage MOS offers a low Ioff current (1nA) but reduced Ion current (550µA) as compared to the high speed MOS

In figure 3-xxx, the low leakage MOS device (left side) has an Ioff current reduced nearly by a factor 100, thanks to a higher threshold voltage (0.4V rather than 0.3V) and larger effective channel length (120nm) compared to the high speed MOS (100nm, see figure 3-xxx). By default, the MOS device is in low leakage option, to encourage low power design. The Ion difference is around 30%. This means that an high speed MOS device is 30% faster than the low leakage MOS. Its use is justified in circuits where speed is critical.

High speed MOS devices may be found in clock trees, data bus interfaces, central processing units, while low leakage MOS are used whenever possible, for all nodes where a maximum switching speed is not mandatory.
**Mos options in Microwind**

A specific layer, called option layer, is used to configure the MOS device option. The layer is situated in the upper part of the palette of layers. The bird's view of the standard MOS is identical to the high speed MOS, except the added option layer which surrounds the MOS device. The p-channel MOS device includes an option layer together with the n-well layer, as seen in figure 3-xxx.

![Option layer used to configure the MOS option](image)

*Fig. 3-xxx: High speed and Low leakage MOS layout. The only difference is the option layer configured for the low leakage option*

An "Ultra-high speed" MOS has been introduced, together with the 90nm technology. This MOS device has a very narrow channel, nearly half of the technology, which increases significantly the Ion current at the price of a very high Ioff parasitic leakage current (Figure 3-xxx).
Fig. 3-xxx: Three types of MOS with different threshold voltage VTO are available in 90nm technology.

**High Voltage MOS**

Integrated circuits with low voltage internal supply and high voltage I/O interface are getting common in deep sub-micron technology. The internal logic of the integrated circuit operates at very low voltage (Typically 1.0V in 0.12µm), while the I/O devices operate in standard voltages (2.5, 3.3 or 5V).

Figure 3-xxx shows the evolution of the supply voltage with the technology generation. The internal supply voltage is continuously decreasing. For compatibility reasons, the chip interface is keep at standard voltages, depending on the target application. Consequently, the input/output structures work at high voltage thanks to specific MOS devices with thick oxide called "High Voltage MOS", while the internal devices work at low voltage for optimum performances.

Fig. 3-xxx: The technology scale down leads to decreased core supply while keeping I/O interfacing compatible with 5V, 3.3V and 2.5V standards
For I/Os operating at high voltage, the high voltage MOS devices are commonly used. High-speed or low leakage devices would be dangerous to use because of their ultra-thin oxide: a 3V voltage applied to the gate of a core MOS device would damage the poly/substrate oxide. The high voltage MOS is built using a thick oxide, two to three times thicker than the low voltage MOS, to handle high voltages as required by the I/O interfaces. Furthermore, the length of the channel is 0.25µm minimum, that is twice the minimum length of core MOS. The cross-section of the three types of MOS (Low leakage, high speed and high voltage) is given in figure 3-xxx.

Fig. 3-xxx: Process section of the high speed and high voltage MOS devices

Fig. 3-xxx. The cross-section of the 3 n-channel MOS options: standard, high speed, and high voltage (liddExplain.MSK)
The I/V Characteristics of the high voltage MOS are plotted in figure 3-xxx, for \( V_{gs} \) and \( V_{ds} \) up to 2.5V. The channel length is 0.25\( \mu \)m and the channel width is 1.2\( \mu \)m. Due to a large channel length, the current drive is less efficient.

There are two main reasons to keep a low-voltage supply for the core of the integrated circuit. The first one is low-power consumption, which is of key importance for integrated circuits used in cellular phones or any...
portable devices. Low supply strongly reduces power consumption by reducing the amplitude of signals, thus reducing the charge and discharge of each elementary node of the circuit. The equation 3-xxx gives an approximation of the power consumption. We deduce that even a small reduction of Vdd has a very positive impact on the reduction of the power consumption.

\[ P = k.C.f.V_{dd}^2 \]  

(Equ. 3-xxx)

where

- \( P \) = power consumption (Watts)
- \( k \) = technology factor, close to 0.5
- \( C \) = total active capacitance of electrical nodes (F) (Not taking into account decoupling capacitance)
- \( f \) = operational frequency of the integrated circuit (Hz)
- \( V_{dd} \) = supply voltage (V)

**Oxide Breakdown**

The second reason for internal low voltage operation is the oxide breakdown. Increased switching performances have been achieved by a continuous reduction of the gate oxide thickness. In 0.12\( \mu \)m technology, the MOS device has an ultra thin gate oxide, around 0.002\( \mu \)m, that is 2nm or 20 Å. Knowing that the molecular distance of SiO2 oxide is around 2 Å, 20 Å means 10 atoms. The oxide may be destroyed by a voltage higher than a maximum limit, called oxide breakdown voltage. A first order estimation is 0.1V/Å [Wang]. Consequently, in 0.12\( \mu \)m, the breakdown voltage is around 2.0V, that is less than twice the nominal VDD (1.2V). An illustration of the breakdown voltage is proposed in figure 3-xxx. If we display the Id/Vd characteristics with Vg higher than VDD, (for example 2.5V instead of 1.2V), the oxide damage is represented by dotted lines (Here for Vg>2.0V). The MOS polarization should always be fixed in such a way that the gate voltage is lower than the breakdown voltage limit.
The oxide may be damaged by a 2V gate voltage. If the gate voltage is further increased, the physical destruction of the oxide may be observed, which result usually in a permanent conductive path between the gate and the source.

**Microwind Configuration**
A set of specific parameters are used for each MOS option to configure the BSIM4 and LEVEL3 models. The industrial approach usually consists in describing each MOS device as a completely separated set of model parameters. Consequently, MOS model cards may include several thousands of parameters. Our approach is guided by an educational and a simplification point of view, at the cost of a poor matching between measured and simulated MOS characteristics. In table 3-xxx, the list of main varying parameters includes the gate oxide, the effective channel length parameter, and the threshold voltage.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>NMOS value in 0.12(\mu \text{m})</th>
<th>NMOS value in 0.12(\mu \text{m})</th>
<th>Name in RUL file</th>
</tr>
</thead>
<tbody>
<tr>
<td>TOX</td>
<td>Gate oxide thickness (low leakage)</td>
<td>20Å</td>
<td>20Å</td>
<td>B4TOX</td>
</tr>
<tr>
<td></td>
<td>(high speed)</td>
<td>20</td>
<td>20</td>
<td>B4T2OX</td>
</tr>
<tr>
<td></td>
<td>(high voltage)</td>
<td>70</td>
<td>70</td>
<td>B4T3OX</td>
</tr>
<tr>
<td>LINT</td>
<td>Channel-length offset parameter (low leakage)</td>
<td>0.0 nm</td>
<td>0.0 nm</td>
<td>B4LINT</td>
</tr>
<tr>
<td></td>
<td>(high speed)</td>
<td>10</td>
<td>10</td>
<td>B4L2INT</td>
</tr>
<tr>
<td></td>
<td>(high voltage)</td>
<td>0.0</td>
<td>0.0</td>
<td>B4L3INT</td>
</tr>
<tr>
<td>VTHO</td>
<td>Long channel threshold voltage (low leakage)</td>
<td>0.40 V</td>
<td>0.40 V</td>
<td>B4VTHO</td>
</tr>
<tr>
<td></td>
<td>(high speed)</td>
<td>0.30</td>
<td>0.30</td>
<td>B4V2THO</td>
</tr>
<tr>
<td></td>
<td>(high voltage)</td>
<td>0.50</td>
<td>0.50</td>
<td>B4V3THO</td>
</tr>
</tbody>
</table>

Table 3-xxx: BSIM4 parameters variation depending on the MOS option

6. Process Variations

The simulated results should not be considered as absolute values. Due to unavoidable process variations during the hundreds of chemical steps for the fabrication of the integrated circuit, the MOS characteristics are never exactly identical from one device to another, and from one die to another. It is very common to measure 5% to 20% electrical difference within the same die, and up to 30% difference between separate dies. One varying parameter is the effective channel length. In figure 3-xxx, although both devices have been designed with a drawn 2 lambda, the result is a 0.11\(\mu \text{m}\) length for the MOS situated on the left side, and 0.13\(\mu \text{m}\) for the MOS situated on the right side.
The same MOS device may be fabricated with an important effective channel variation.

If we cumulate several measurements on a wide number of devices, we can plot the probability of occurrence versus the measured effective length. The curve is usually a normal distribution with a center close to the default parameter given in the electrical rules.

**Simulation with Microwind**

The menu **Simulate → Simulation parameters** gives a simple access to minimum/typical/maximum parameter sets (Figure 3-xxx). The industrial approach usually consists in providing a separate set of model parameters for each case, which represents a huge amount of model parameters. In Microwind, the approach has consisted in altering two main parameters: the threshold voltage (20% variation) and the mobility (20% variation). All other parameters are supposed to be constant.
A comparative simulation of the Id/Vd curve in typical, maximum and minimum scenarios shows a very large variation of performances. The user may automatically switch from one parameter set to another by a press of a key ("M" for maximum, "m" for minimum, "t" for typical).

---

**Fig. 3-xxx: The MOS Id/vd curve in Min,Typ,Max modes.**
To superimpose the three curses, click the small brain icon (Enable Memory), and increase the "Step Vg" to 1.2 to draw only one curve for each mode. Notice the important variation between the minimum Ion and maximum Ion (From 125µA to 200µA). In reality, the MOS characteristics vary in a normal distribution around the typical case. Consequently, the Ion current of this MOS device has a strong probability to reach the typical value. The min/max simulation is very interesting to validate the design in extreme situations. The min/max simulation should also consider the temperature: the worst current is obtained at high temperature, minimum set of parameters, while the highest current is obtained at low temperature, maximum set of parameters.

7. Concluding remarks

The number of parameters required for various MOS models is reported in figure 3-xxx. It can be seen that the trend is to increase the number of parameters, in order to take in account various effects linked to the device scale down.

![Increased number of parameters in the MOS models](image)

Even with advanced models, the resulting models may not fit well in all operating regions, for all device sizes. This is why the industrial approach for building model parameters is based on optimization mathematical algorithms. In deep submicron technology, the model parameters have a strong variation with the device size. For example the threshold voltage and mobility vary significantly with the device length, and the equations cannot handle always properly this dependencies. One solution is called binning. It consists in breaking the width-length space into several regions, as illustrated in figure 3-xxx. In each region, a specific set of model parameters is setup and optimized.
Binning severely complicates the process of parameters extraction. In the case of figure 3-xxx, 6 sets of parameters are required. Notice that the set 1 covers small length and small width. The set n°2 covers a wider length interval, while set n°3 is valid for any length greater than 1µm. This is because long length devices are easier to model than short length devices, where many second order effects appear. Binning is used in industry to increase the analog simulation accuracy, at the cost of several drawbacks: the simulation time cost due to model complexity, and discontinuities in the current prediction that may be observed at the boundary of two sets. These limitations are the fuel for constructing more complex models that fit well for the whole range of width and length. In the future nano-scale technologies may require MOS models with up to 1000 parameters, requiring a degree of expertise never attained up to now.

REFERENCES

[Bsim4] BSIM4 web site www-device.eecs.berkeley.edu

EXERCISES

<To be added>