ML506 DSP Hardware Co-Simulation with Xilinx System Generator for DSP 10.1i SP2

August 2008
ML506 Overview

- ML506 Board
- Setup
  - Software Requirements
  - Network Setup
  - Hardware Setup
  - CompactFlash Setup
- System Generator Hardware Co-Simulation
- Available Documentation
ML506 Board

USB Peripheral - J17
Serial Port COM2
Line Out - P12
Line In - P11
Microphone In - P10
Power Connector, P20
Power-On Switch SW1
Diff CLK Out J12, J13
Piezo Transducer SW1

Virtex-5 XC5VSX50T FPGA

Rotary Switch SW3

USB Host, J18
SFP Module, P19
SPDIF Out, P14
Parallel Cable IV (PC4) JTAG, J1
VGA Port P8
MGT Connection J42-J45
Ethernet P6
Diff CLK In J10, J11
Digital Video Connector, P7

SATA Connectors J40, J41
Prog Pushbutton, SW5 SYSACE Reset, SW4 CPU Reset, SW7

PCIe Interface
Status & Error LEDs
GPIO LEDs
GPIO PBs
GPIO DIP SW8

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Additional Setup Details

• Refer to ml505_overview_setup document for details on:
  – Software Requirements
  – ML505 Board Setup
    • Equipment and Cables
    • Software
    • Network
  – Terminal Programs
    • This presentation requires the 9600-8-N-1 Baud terminal setup

Note: The ML505 overview presentation covers the ML506 board
ISE Software Requirement

- Xilinx ISE 10.1i SP2 software
CORE Generator Requirement

- Xilinx CORE Generator 10.1i IP Update 2
Sysgen Software Requirement

- Xilinx Sysgen 10.1i

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Note: Presentation applies to the ML506
Matlab Software Requirement

• Matlab is a third party software, available from Mathworks
  – Matlab R2008a

Note: Presentation applies to the ML506
WinPcap Software Requirement

• As stated in the System Generator User’s Guide, pg. 215, WinPcap is required for Co-simulation
  – [www.winpcap.org](http://www.winpcap.org) Version 4.0 or higher
Network Setup

- A Gigabit Ethernet Adapter on your PC is required
- In the Network Connections, right-click on the Ethernet Adapter and select Properties (1)
Network Setup

- Set your host (PC) to this IP Address:

Note: Presentation applies to the ML506
Network Setup

- Click Configure (1)
  - Set the Flow Control to Auto

Note: Presentation applies to the ML506
Network Setup

- Set Speed & Duplex to Auto
Network Setup

• Set the Ethernet PHY jumper settings
  – This presentation requires GMII/MII
  – Set J22, J23 to positions 1-2 (as shown)
Network Setup

- Connect an Ethernet cable from the ML506 to the PC’s Ethernet Adapter

Note: Presentation applies to the ML506
Software Setup

- Select Start → All Programs → Xilinx ISE Design Suite 10.1 → DSP_Tools → Select MATLAB version for Xilinx System Generator
- Select Matlab version R2008a

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Software Setup

- Select Start → All Programs → Xilinx ISE Design Suite 10.1 → DSP_Tools → Xilinx System Generator 10.1
Hardware Setup

- Use a CompactFlash reader to mount a CompactFlash as a disk drive
- Delete all files in this CompactFlash
Hardware Setup

• Open Matlab and type this command to update the CompactFlash:
  
  ```matlab
  unzip(fullfile(xlFindSysgenRoot,'plugins/bin/ML506_sysace_cf.zip'), '<CF Drive Letter>:\')
  ```
Hardware Setup

- These files should appear on your CompactFlash
- Eject the CompactFlash from your PC
CompactFlash Setup

- Insert the CompactFlash fully into the CompactFlash slot on the ML506 board
Hardware Setup

- Set Front DIP Switches to 10010101
- Power on the ML506

Note: In some cases, you may need to press the CPU reset if the network doesn’t connect
Open DSP Example

- From Matlab R2006b, select Help → Demos

Note: Presentation applies to the ML506
Open DSP Example

- Select Blocksets → Xilinx → More demos and Examples → Local Examples (1) and click on the User’s Guide link (2)

Note: Presentation applies to the ML506
Open DSP Example

- Scroll down to the DSP section and select the FIR filter using the DSP48 Macro block and click on “Open this model” (1)
DSP48 Macro

- Model appears as seen below

Note: If this file is write protected, save as a new name or make it writable
Move the input

- Click once on the net marked “Input” and press the delete key
Move the input

- The net from the Sine wave to the adder input should still be connected.
Move the input

- Drag a connection from the scope (1) to the net after the adder (2)
Move the input

- Double click this new net and name it “Input_with_Noise” (1)
Generate Block

- Right click the System Generator Block and select Open Block (1)

Note: Presentation applies to the ML506
Generate Block

- Select Compilation: Hardware Co-simulation > ML506 > Ethernet > Point-to-point (1)

Note: Presentation applies to the ML506
Generate Block

- Click Generate (1)

Note: Presentation applies to the ML506
Generated DSP48 Block

- After compilation, a new window with the generated DSP Hardware block appears
  - Note: The order of the output pins varies from the top to bottom order in the model; pay attention to this when making connections
Add DSP48 Block

- Drag block from library window to original dsp48 window

Note: Presentation applies to the ML506
Add DSP48 Block

- Click on the Simulink button in Matlab

Note: Presentation applies to the ML506
Add DSP48 Block

- In the Simulink Library Browser under Simulink → Discrete, right click on the Discrete filter and add it to the dsp48macro_macfir
- Also add an Integer Delay, a Scope, and two Sum blocks

Note: The Scope and Sum blocks can be found under Commonly Used Blocks
Configure Scope

- Double-click on Scope1, click the parameters button (1) and set the number of Axes to 6 (2)

Note: The Scope and Sum blocks can be found under Commonly Used Blocks.
Configure Scope

- Double-click on Discrete Filter1, set the numerator coefficient to \texttt{fir1(15,0.5)}, and the Denominator coefficient to 1
Configure Scope

- Double-click on Sum3 and Sum4 blocks, and set the list of signs to |+-|

Note: Presentation applies to the ML506
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Run Hardware Co-simulation

- Double click on the dsp48macro_macfir hwcosim block
Run Hardware Co-simulation

- Under the Ethernet tab, select the desired Ethernet Connection

Note: Presentation applies to the ML506
Run Hardware Co-simulation

• Under the Configuration tab, select Point-to-point Ethernet
  – Click OK
Output Waveforms

• Right Click on Scope and select **Open Block**
• Repeat for Scope1
• Both should show no waveforms
• Click **Dock Scope** (small down arrow) on both (1)
Output Waveforms

- In the Matlab window, click Undock Figures (small up arrow) (1)
Output Waveforms

- Figures Window set to side-by-side display
Simulate the FIR Filter

The modified n-tap MAC FIR Filter block can run at a speed of up to 450MHz. This cannot be met by the n-tap Mac FIR filter block that does not use DSP48.

Note: Presentation applies to the ML506
Output Waveforms

- Click Autoscale for both scopes (1)
- The waveforms should be identical

Note: Presentation applies to the ML506
Documentation

- **Virtex-5**
  - Silicon Devices
  - Virtex-5 Multi-Platform FPGA
  - Virtex-5 Family Overview: LX, LXT, SXT, and FXT Platforms
  - Virtex-5 FPGA DC and Switching Characteristics Data Sheet
Documentation

• Virtex-5
  – Virtex-5 FPGA User Guide  
  – Virtex-5 FPGA Configuration User Guide  
  – Virtex-5 System Monitor User Guide  
  – Virtex-5 Packaging and Pinout Specification  
Documentation

- Virtex-5 RocketIO
  - RocketIO GTP Transceivers
  - RocketIO GTX Transceivers
  - RocketIO GTP Transceiver User Guide – UG196
  - RocketIO GTX Transceiver User Guide – UG198
Documentation

• Design Resources
  – ISE Development Tools and IP
    http://www.xilinx.com/ise
  – Integrated Software Environment (ISE) Foundation Resources
    http://www.xilinx.com/ise/logic_design_prod/foundation.htm
  – ISE Manuals
    http://www.xilinx.com/support/software_manuals.htm
  – ISE Development System Reference Guide
  – ISE Development System Libraries Guide
    http://toolbox.xilinx.com/docsan/xilinx10/books/docs/virtex5_hdl/virtex5_hdl.pdf
Documentation

• Additional Design Resources
  – Customer Support
    http://www.xilinx.com/support
  – Xilinx Design Services:
    http://www.xilinx.com/xds
  – Titanium Dedicated Engineering:
    http://www.xilinx.com/titanium
  – Education Services:
    http://www.xilinx.com/education
  – Xilinx On Board (Board and kit locator):
    http://www.xilinx.com/xob
Documentation

- Platform Studio
  - Embedded Development Kit (EDK) Resources
    http://www.xilinx.com/edk
  - EDK Concepts, Tools, and Techniques
Documentation

- PowerPC 440
  - PowerPC 440 Processor
    [Link](http://www.xilinx.com/powerpc)
  - Embedded Processor Block in Virtex-5 FPGAs Reference Guide – UG200
    [Link](http://www.xilinx.com/support/documentation/user_guides/ug200.pdf)
  - PPC440 Virtex-5 Wrapper – DS621
    [Link](http://www.xilinx.com/support/documentation/ip_documentation/ppc440_virtex5.pdf)
  - DDR2 Memory Controller for PowerPC 440 Processors – DS567
    [Link](http://www.xilinx.com/support/documentation/data_sheets/ds567.pdf)
Documentation

• MicroBlaze
  – MicroBlaze Processor
    http://www.xilinx.com/microblaze
  – MicroBlaze Processor Reference Guide – UG081
Documentation

• ChipScope Pro
  – ChipScope Pro 10.1i Serial IO Toolkit User Manual
    http://www.xilinx.com/ise/verification/chipscope_pro_siotk_10_1_ug213.pdf
  – ChipScope Pro 10.1i ChipScope Pro Software and Cores User Guide
    http://www.xilinx.com/ise/verification/chipscope_pro_sw_cores_10_1_ug029.pdf
Documentation

• Memory Solutions
  – Demos on Demand – Memory Interface Solutions with Xilinx FPGAs
    http://www.demosondemand.com/clients/xilinx/001/page_new2/index.asp#35
  – Xilinx Memory Corner
    http://www.xilinx.com/products/design_resources/mem_corner
  – Additional Memory Resources
  – Xilinx Memory Interface Generator (MIG) 2.1 User Guide
  – Memory Interfaces Made Easy with Xilinx FPGAs and the Memory Interface Generator
Documentation

• Ethernet
  – Virtex-5 Embedded Tri-Mode Ethernet MAC Wrapper Data Sheet
  – Virtex-5 Embedded Tri-Mode Ethernet MAC Wrapper Getting Started Guide
  – Virtex-5 Tri-Mode Ethernet Media Access Controller User Guide
  – LightWeight IP (lwIP) Application Examples – XAPP1026
Documentation

• PCIe
  – LogiCORE Endpoint Block Plus for PCI Express Data Sheet
    http://www.xilinx.com/support/documentation/ip_documentation/
    pcie_blk_plus_ds551.pdf
  – LogiCORE Endpoint Block Plus for PCI Express Designs
    http://www.xilinx.com/support/documentation/ip_documentation/
    pcie_blk_plus_ug341.pdf
  – LogiCORE Endpoint Block Plus Getting Started Guide for PCI Express Designs
    http://www.xilinx.com/support/documentation/ip_documentation/
    pcie_blk_plus_gsg343.pdf
  – Virtex-5 Integrated Endpoint Block User Guide for PCI Express Designs
Documentation

• System Generator
  – System Generator for DSP
  – Xilinx System Generator for DSP User Guides
  – XtremeDSP Design Considerations
Documentation

• PLB v4.6 IP
  – Processor Local Bus (PLB) v4.6 Data Sheet – DS531
  – Multi-Port Memory Controller (MPMC) – DS643
  – XPS Multi-CHannel External Memory Controller (XPS MCH EMC) – DS575
  – XPS LocalLink TEMAC – DS537
  – XPS LocalLink FIFO – DS568
Documentation

• PLB v4.6 IP
  – XPS IIC Bus Interface – DS606
  – XPS SYSACE (System ACE) Interface Controller – DS583
  – XPS Timer/Counter – DS573
  – XPS Interrupt Controller – DS572
  – Using and Creating Interrupt-Based Systems Application Note
Documentation

• PLB v4.6 IP
  – XPS General Purpose Input/Output (GPIO) – DS569
  – XPS External Peripheral Controller (EPC) – DS581
  – XPS 16550 UART – DS577
  – PLBV46 to DCR Bridge Data Sheet – DS578
Documentation

- IP
  - Local Memory Bus Data Sheet – DS445
  - Block RAM Block Data Sheet – DS444
  - Microprocessor Debug Module Data Sheet – DS641
  - LMB Block RAM Interface Controller Data Sheet – DS452
  - Device Control Register Bus (DCR) v2.9 Data Sheet – DS406
Documentation

- IP
  - JTAGPPC Controller Data Sheet – DS298
  - Processor System Reset Module Data Sheet – DS402
  - Clock Generator v2.0 Data Sheet – DS614
  - Util Bus Split Operation Data Sheet – DS484
Documentation

- ML505/506/507
  - ML505 Overview
    http://www.xilinx.com/ml505
  - ML506 Overview
    http://www.xilinx.com/ml506
  - ML507 Overview
    http://www.xilinx.com/ml507
  - ML505/506/507 Getting Started Tutorial – UG348
Documentation

- ML505/506/507
  - ML505/506/507 Schematics
    http://www.xilinx.com/support/documentation/boards_and_kits/ml50x_schematics.pdf
  - ML505/506/507 Bill of Material
    http://www.xilinx.com/support/documentation/boards_and_kits/ml505_501_bom.xls